CLAIMS

What is claimed is:

1. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project a height above said active surface;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry;

applying an encapsulant material at least over said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements; and

removing a depth of said encapsulant material sufficient to expose a portion of each of said intermediate conductive elements.

2. The method of claim 1, further comprising forming external conductive elements over said exposed portions of said intermediate conductive elements.

3. The method of claim 1, further comprising severing said semiconductor substrate in alignment with at least some of said channels into a plurality of semiconductor elements, each semiconductor element comprised of at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material.

4. The method of claim 1, further comprising forming said channels with sloped side walls defining opposing chamfers.

5. The method of claim 4, further comprising forming said channels by sawing or a substantially isotropic etch.

6. The method of claim 1, further comprising forming said channels with substantially parallel side walls.

7. The method of claim 6, further comprising forming said channels using a laser or a substantially anisotropic etch.

8. The method of claim 1, further comprising applying said encapsulant material to said active surface by transfer molding.

9. The method of claim 1, further comprising dispensing said encapsulant material over said active surface.

10. The method of claim 1, wherein said removing said encapsulant material is effected by abrasive planarization.

11. The method of claim 1, wherein forming said intermediate conductive elements is effected by forming solder balls.

12. The method of claim 1, wherein forming said intermediate conductive elements is effected by forming pillars of a conductive or conductor-filled epoxy or a metal-filled elastomer.

13. The method of claim 1, wherein forming said intermediate conductive elements is effected by a wire bonding capillary.

14. The method of claim 2, wherein forming said external conductive elements comprises forming solder balls.

15. The method of claim 2, wherein forming said external conductive elements comprises forming pillars of a conductive or conductor-filled epoxy.

16. The method of claim 2, wherein forming said external conductive elements comprises applying an anisotropically conductive film over said encapsulant material.

17. The method of claim 1, further comprising forming said encapsulant material from a material selected from the group comprising filled polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes and glasses.

18. The method of claim 1, further comprising forming a layer of encapsulant material on a back side of said semiconductor substrate.

19. The method according to claim 1, comprising:
placing said semiconductor substrate with said intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and
electrically connecting said intermediate conductive elements and said conductive bumps.

20. The method of claim 19, further including forming bond pads over the exposed portions of said intermediate conductive elements before electrically connecting said intermediate conductive elements to said conductive bumps.

21. The method according to claim 3, comprising:
placing at least one of said semiconductor elements with said intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and
electrically connecting said intermediate conductive elements and said conductive bumps.

22. The method of claim 21, further including forming bond pads over the exposed portions of said intermediate conductive elements before electrically connecting said intermediate conductive elements to said conductive bumps.

23. The method of claim 2, further comprising severing said semiconductor substrate in alignment with at least some of said channels into a plurality of semiconductor elements, each semiconductor element comprised of at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material.

24. The method of claim 23, comprising:

placing at least one of said semiconductor elements with said external conductive elements in alignment with terminal pads of a carrier substrate; and

electrically connecting said external conductive elements and said terminal pads.

25. The method of claim 2, further comprising placing said semiconductor substrate with said external conductive elements in alignment with terminal pads of a carrier substrate and electrically connecting said external conductive elements to said terminal pads.

26. The method of claim 1, further comprising forming conductive traces over said encapsulant material from said exposed portions of said intermediate conductive elements to at least one channel of said pattern of channels, defining a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced edge contacts therealong, and severing said semiconductor substrate in alignment with at least some of said channels including said at least one channel into a plurality of semiconductor elements comprised of at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material and said plurality of laterally spaced edge contacts are located along a peripheral edge of a semiconductor element of the plurality.

27. The method of claim 26, further comprising aligning said plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the edge contacts with the edge connectors.